INTEGRATED PHOTO FLASH CHARGER AND IGBT DRIVER

FEATURES

- **Highly Integrated Solution to Reduce Components**
- **Integrated 50-V Power Switch, $R_{(ON)}$ = 200 mΩ Typical**
- **Integrated IGBT Driver**
- **High Efficiency**
- **Programmable Peak Current, 0.95 A ~ 1.8 A**
- **Input Voltage of 1.8 V to 12 V**
- **Optimized Control Loop for Fast Charge Time**
- **Sensing All Trigger From Primary Side**
- **10-Pin MSOP/16-Pin QFN Package**
- **Protection**
  - **– MAX On Time**
  - **– Over V_{DS} Shutdown**
  - **– Thermal Monitor**

APPLICATIONS

- **Digital Still Cameras (DSC)**
- **Optical Film Cameras**
- **Mobile Phones With Camera**
- **PDAs With Camera**

DESCRIPTION

This device offers a complete solution for charging a photo flash capacitor from battery input, and subsequently discharging the capacitor to the xenon tube. The device has an integrated power switch, IGBT driver, and control logic blocks for charge applications. Compared with discrete solutions, the device significantly reduces the component count, shrinks the solution size, and eases design complexity. Additional advantages are fast charging time and high efficiency due to the optimized PWM control algorithm.

Other provisions of the device includes four options for determining a different target voltage, programmable peak current, thermal disable monitor, input signal for charge enable, flash enable, and an output signal for charge completion status.

PRODUCT PREVIEW

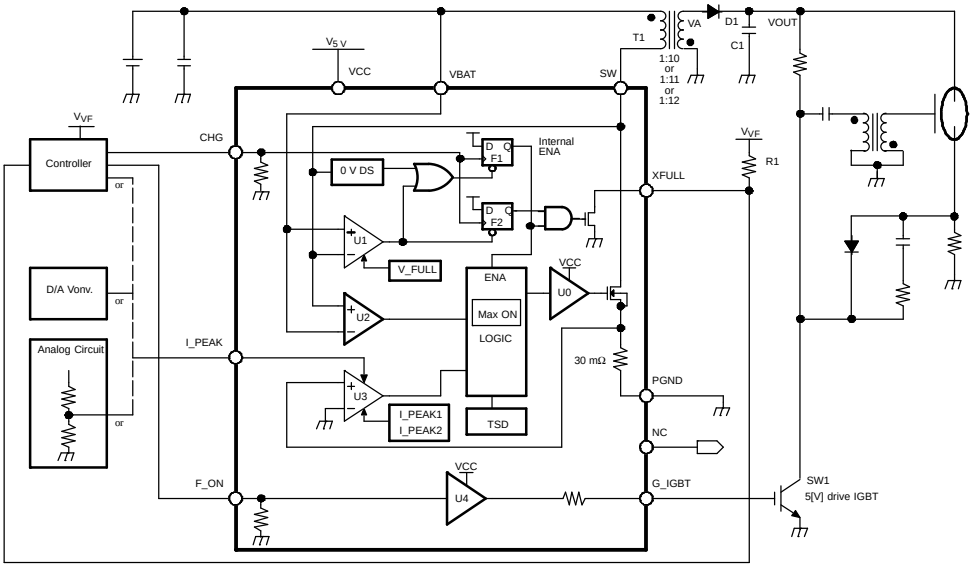


Figure 1. Typical Application Circuit(1)

(1) TI assumes no responsibility for the consequences of use of this application circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	TARGET VOLTAGE at PRIMARY SIDE	PACKAGE MARKING	PACKAGE	PART NUMBER
-35°C to 85°C	29	BKV	16-pin QFN	TPS65552ARGT
-35°C to 85°C	29	BMA	10-pin MSOP	TPS65552ADGQ

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			UNIT
V_{SS}	Supply voltage	VCC	-0.6 V to 6 V
		VBAT	-0.6 V to 13 V
$V_{(SW)}$	Switch terminal voltage		-0.6 V to 50 V
	Switch current between SW and PGND, ISW		3 A
V_I	Input voltage of CHG, I_PEAK, F_ON		-0.3 V to V_{CC}
T_{stg}	Storage temperature		-40°C to 150°C
T_J	Maximum junction temperature		125°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage, VCC	4.5		5.5	V
	Supply voltage, VBAT	1.8		12	V
$V_{(SW)}$	Switch terminal voltage,	-0.3		45	V
	Switch current between SW and PGND			2	A
	Operating free-air temperature range	-35		85	°C
V_{IH}	High-level digital input voltage at CHG and F_ON	2.4			V
V_{IL}	Low-level digital input voltage at CHG and F_ON			0.6	V

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$ (1)	POWER RATING T_A < 25°C	POWER RATING T_A = 70°C	POWER RATING T_A = 85°C
MSOP	49.08 °C/W	2.04 W	1.12 W	815 mW
QFN	47.40 °C/W	2.11 W	1.16 W	844 mW

(1) The thermal resistance, $R_{\theta JA}$, is based on a soldered PowerPAD™ on a 2S2P JEDEC board using thermal vias.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

T_A = 25°C, VBAT = 4.2 V, VCC = 5 V, $V_{(SW)}$ = 4.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(ONL)}$	ON resistance of XFULL	$I_{(XFULL)}$ = -1 mA		1.5	3	kΩ
$V_{(PKH)}$ (1)	Upper threshold voltage of I_PEAK		2.4			V
$V_{(PKL)}$ (1)	Lower threshold voltage of I_PEAK				0.6	V
I_{CC1}	Supply current from VBAT	CHG = H, $V_{(SW)}$ = 0 V (free run by t_{MAX})		27		µA
I_{CC2}	Supply current from VCC	CHG = H, $V_{(SW)}$ = 0 V (free run by t_{MAX})		2.5	5	mA
I_{CC3}	Supply current from VCC and VBAT	CHG = L			1	µA
I_{lkg1}	Leakage current of SW terminal				2	µA
I_{lkg2}	Leakage current of XFULL terminal	$V_{(XFULL)}$ = 5 V			1	µA
$R_{(ONSW)}$	SW ON resistance between SW and PGND	$I_{(SW)}$ = 1 A		0.3	1	Ω
$R_{(IGBT1)}$	G_IGBT pullup resistance	$V_{(G\_IGBT)}$ = 0 V	5	10	15	Ω
$R_{(IGBT2)}$	G_IGBT pulldown resistance	$V_{(G\_IGBT)}$ = 5 V	25	51	75	Ω
$I_{(PEAK1)}$	Upper peak of $I_{(SW)}$	$V_{(I\_IPEAK)}$ = 3 V	1.58	1.68	1.78	A
$I_{(PEAK2)}$	Lower peak of $I_{(SW)}$	$V_{(I\_IPEAK)}$ = 0 V	0.77	0.87	0.97	A
$V_{(FULL)}$	Charge completion detect voltage at $V_{(SW)}$	TPS65552A	28.7	29	29.3	V
$V_{(ZERO)}$	Zero current detection at $V_{(SW)}$		1	20	60	mV
$T_{(SD)}$ (1)	Thermal shutdown temperature		150	160	170	°C
	Over V_{DS} detection at $V_{(SW)}$		0.95	1.2	1.45	V
t_{MAX}	MAX ON time		50	80	120	µs
$R_{(INPD)}$	Pulldown resistance of CHG, F_ON	VCHG = $V_{(F\_ON)}$ = 4.2 V		100		kΩ

(1) Specified by design.

SWITCHING CHARACTERISTICS

T_A = 25°C, VBAT = 4.2 V, VCC = 5 V, $V_{(SW)}$ = 4.2 V (unless otherwise noted)

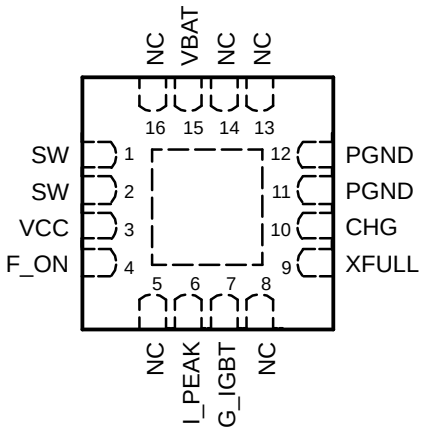
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD} (1)	Propagation delay	F_ON↑↓ - G_IGBT↑↓		50		ns
		SW ON after $V_{(SW)}$ dips from $V_{(ZERO)}$		45		ns
		SW OFF after $I_{(SW)}$ exceeds $I_{(PEAK)}$		270		ns
		XFULL↓ after $V_{(SW)}$ exceeds $V_{(FULL)}$		300		ns
		SW ON after CHG↑		20		ns
		SW OFF after CHG↓		20		ns

(1) Specified by design.

PRODUCT PREVIEW

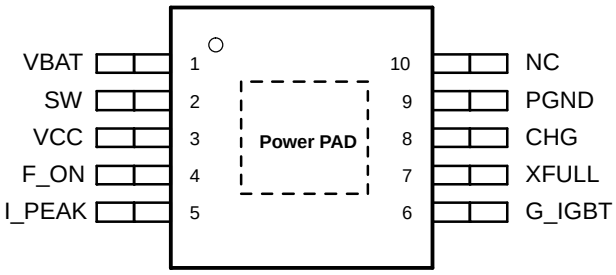
PIN ASSIGNMENT

RGT PACKAGE
(TOP VIEW)



NC − No internal connection

DGQ PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

PIN NUMBER		SIGNAL	I/O	DESCRIPTION
RGT	DGQ			
1, 2	2	SW	O	Primary side switch
3	3	VCC	I	Power supply voltage
4	4	F_ON	I	G_IGBT control input
5, 8, 13, 16	–	NC		No connection (internally open)
6	5	I_PEAK	I	Peak current control input
7	6	G_IGBT	O	IGBT gate driver output
9	7	XFULL	O	Charge completion output
10	8	CHG	I	Charge control input
11, 12	9	PGND		Power ground
14	10	NC		No connection (used by TI, should be open pin)
15	1	VBAT	I	Battery voltage input

PRODUCT PREVIEW

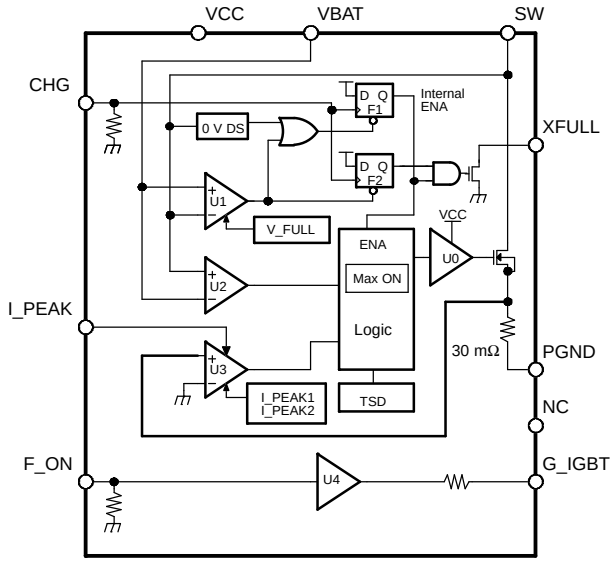


Figure 2. Functional Block Diagram

I/O Equivalent Circuits

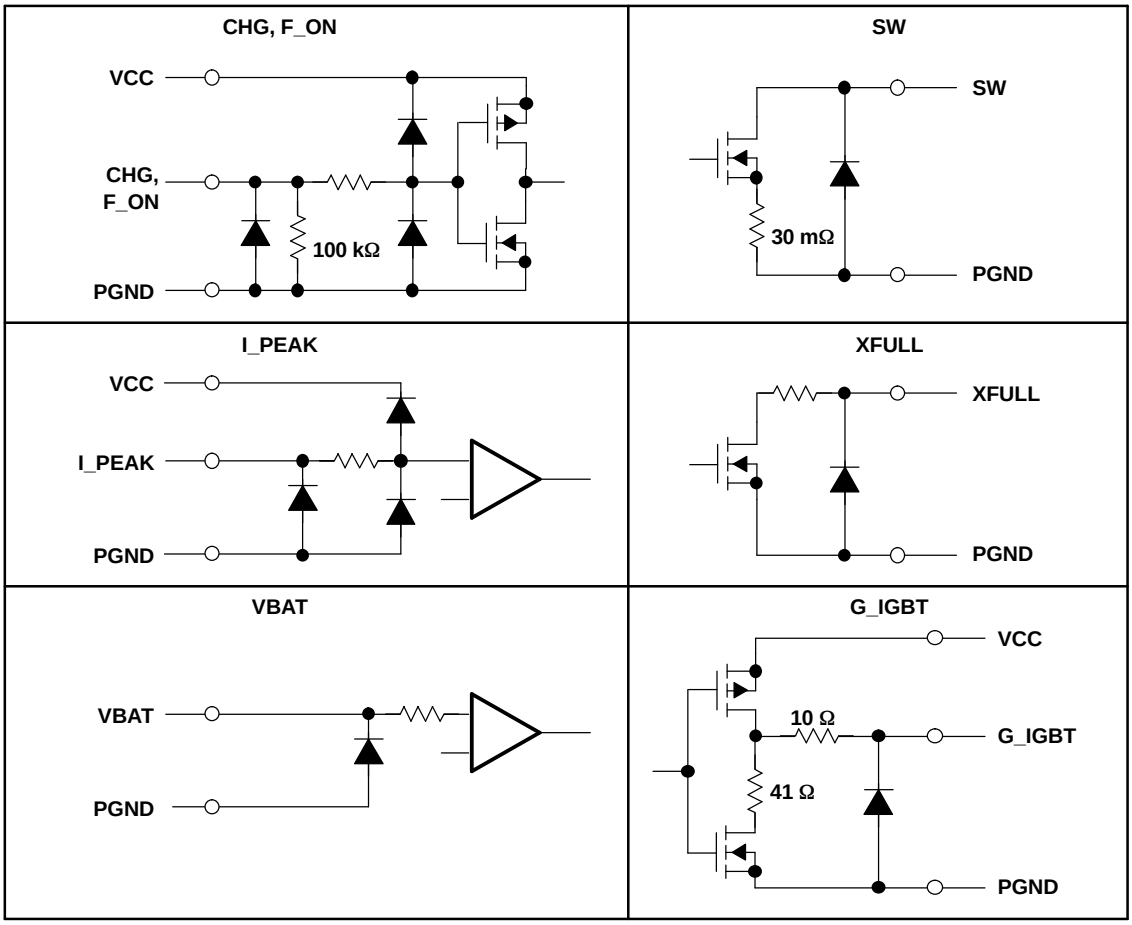


Figure 3. I/O Equivalent Circuits

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

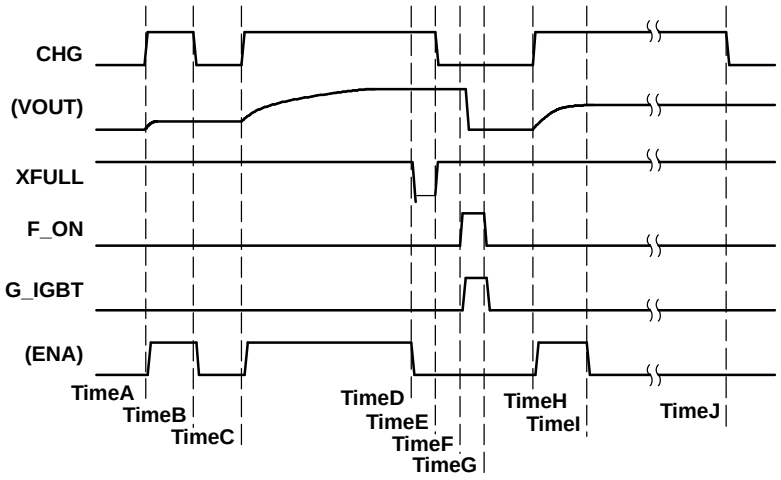


Figure 4. Whole Operation Sequence Chart

Start/Stop Charging

TPS65552A has one internal enable latch, F1, that holds a charge *(ON/OFF* status) of the device. See Figure 2.

The only way to *start* charging is to input CHG↑ (see time A/C/H in Figure 4). Each time CHG↑ is reached, the TPS65552A starts charging.

There are three trigger events to *stop* charging:

1. Forced *stop* by inputting CHG = L from the controller (see timeB in Figure 4).
2. Automatic *stop* by detecting full charge. VOUT reaches the target value (see TimeD in Figure 4).
3. Protected *stop* by over V_{DS} detection (see TimeI in Figure 4).

Indicate Charging Status

When the charging operation is completed, the TPS65552A drives the charge completion indicator pin, XFULL, to GND. XFULL is an open-drain type output. When connecting the indicator LED to XFULL, the LED lights are on when fully charged. The controller detects the status of the device as a logic signal when connecting a pullup resister, R1 (see Figure 1).

XFULL enables the controller to detect the over V_{DS} protection status using software time. If over V_{DS} protection occurs, XFULL never goes L during CHG = H, provided that the timer that starts at CHG↑ stops at XFULL↑, and times out within a designed period of maximum charging times. The controller can detect over V_{DS} at time out.

The device starts charging at *timeH*, and over V_{DS} protection occurs at TimeI (see Figure 4). At timeI, XFULL stays H, and the controller detects over V_{DS} protection when the timer ends at timeJ. In this event, the controller inputs CHG = L to terminate the operation.

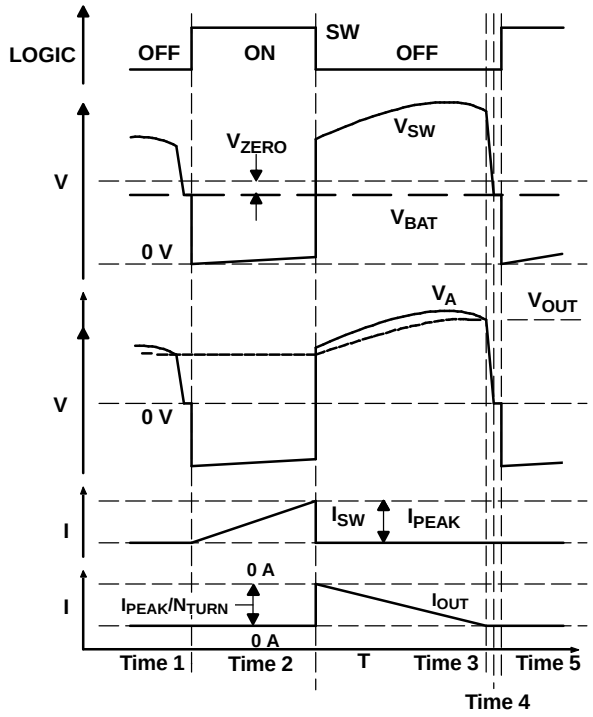


Figure 5. Timing Diagram at One Switching Cycle

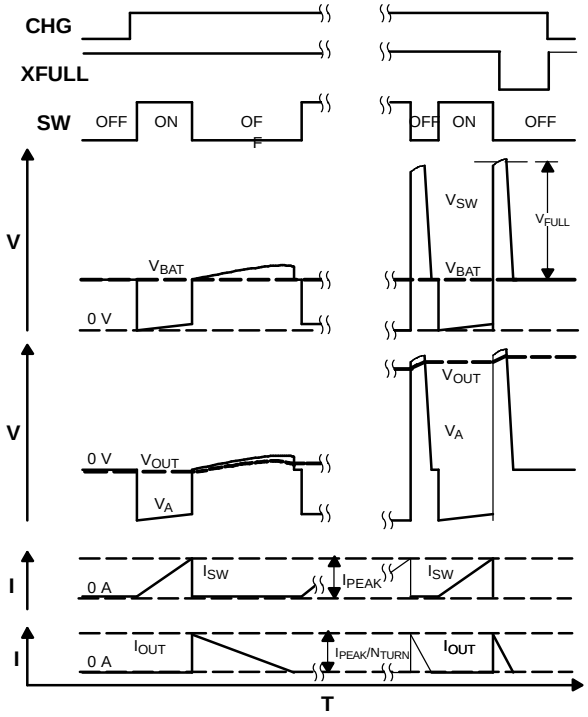


Figure 6. Timing Diagram at Beginning/Ending

Control Charging

The TPS65552A provides three comparators to control charging. Figure 2 shows the block diagram of TPS65552A and Figure 5 shows one timing diagram switching cycle. Note that emphasis is placed on Time1 and Time3 of the waveform in Figure 5.

While SW is ON (Time1 to Time2 in Figure 5), U3 monitors current flow through integrated power-MOSFET from SW to PGND. When $I_{(SW)}$ exceeds $I_{(PEAK)}$, SW turns OFF (Time2 in Figure 5).

When SW turns OFF (Time2 in Figure 5), the magnetic energy in the transformer starts discharging. Meanwhile, U2 monitors the kickback voltage at the SW terminal. As the energy is discharging, the kickback voltage is increasing according to the increase of V_{OUT} (Time2 to Time3 in Figure 5). When almost all energy is discharged, the system cannot continue rectification via the diode, and the charging current of I_{OUT} goes to zero (Times3 in Figure 5). After rectification stops, the small amount of energy left in the transformer is released via the parasitic path, and the kickback voltage reaches zero (Time3 to Time4 in Figure 5). During this period, U2 makes SW turn ON when ($V_{(SW)}$ - VBAT) dips from $V_{(ZERO)}$ (Time5 in Figure 5). In the actual circuit, the period between Time4 and Time5 in Figure 5 is small or does not appear dependent on the delay time of the U2 detection to SW ON.

U1 also monitors the kickback voltage. When ($V_{(SW)}$ - VBAT) exceeds $V_{(FULL)}$, TPS65552A stops charging (see Figure 6).

In Figure 5 and Figure 6, *ON* time is always the same period in every switching. The *ON* time is calculated by Equation 1. This equation is not dependent on output voltage.

$$t_{ON} = L \frac{I_{PEAK}}{V_{BAT}} \quad (1)$$

However, *OFF* time is dependant on output voltage. As the output voltage gets higher, the *OFF* time gets shorter (see Equation 2).

$$t_{OFF} = N\_TURN \times L \frac{I_{PEAK}}{V_{OUT}} \quad (2)$$

Reference Voltage

The TPS65552A does not have its own reference voltage circuit inside, and the TPS65552A uses the VCC input voltage as a reference to detect $I_{(PEAK)}$, $V_{(ZERO)}$, and $V_{(FULL)}$. Therefore, voltage input at VCC is approximately 5 V.

VCC differs from 5 V by system limitations. Table 1 shows the dependence of each function of TPS65552A to VCC.

Table 1. VCC Dependence of TPS65552A

PARAMETER		EQUATION	VCC		
			4.5	5	5.5
$I_{(PEAK1)}$		0.52 x VCC - 0.92	1.42	1.68	1.94
$I_{(PEAK2)}$		0.24 x VCC - 0.33	0.75	0.87	0.99
$V_{(FULL)}$	TPS65552A	5.8 x VCC	26.1	29.0	31.9
	over V_{DS}	0.24 x VCC	1.08	1.2	1.32

Termination Voltage Setting

To obtain a different termination voltage, transformers of different turn ratio are required. Table 2 shows the matrix of termination voltage and the turn ratio of the transformer. The table only shows a *ONE to integer* ratio while there are no limitations for a turn ratio of the transformer in a real application circuit, example 1:10.5 (= 10:105).

Table 2. Termination Voltage Setting Table

	TPS65552A
	29 [V]
1:10	290
1:11	319
1:12	348

Programming Peak Current

The TPS65552A provides a method to program $I_{(PEAK)}$ through the input voltage of the I_PEAK terminal. Figure 7 shows how to program $I_{(PEAK)}$.

I_PEAK input is treated as a logic input, when its voltage is below $V_{(PKL)}$ (0.6 V) and above $V_{(PKH)}$ (2.4 V). Between $V_{(PKL)}$ and $V_{(PKH)}$, I_PEAK input is treated as an analog input. Using this characteristic, $I_{(PEAK)}$ can be set by the logic signal or by an analog input.

Typical usages of this function are:

1. Charging $I_{(PEAK)}$ depends on the battery voltage. Large $I_{(PEAK)}$ for an adequate battery, small $I_{(PEAK)}$ for a poor battery.
2. Reducing $I_{(PEAK)}$ when zooming lens (motor works); this avoids shutdown of the battery with a large current output.

In Figure 1, three optional connections to I_PEAK are shown.

1. Use the controller to treat I_PEAK as the logic input pin. This option is the easiest.
2. Use a D/A converter to force $I_{(PEAK)}$ to follow analog information, such as battery voltage.
3. Use an analog circuit to achieve the same results as the D/A converter.

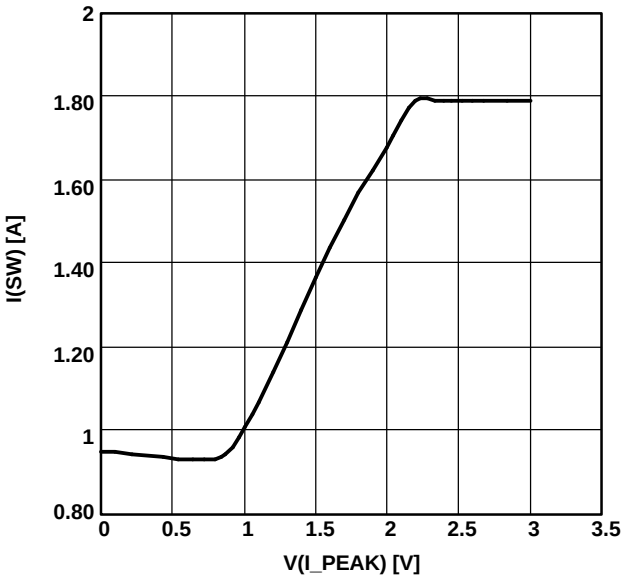


Figure 7. I_PEAK vs $I_{(SW)}$

IGBT Driver Control

The IGBT driver provided by the TPS65552A is a simple buffer in the logical table. Table 3 shows the function (see Figure 4).

Table 3. IBGT Driver Function Table

F_ON	G_IGBT
L	L
H	H

Protections

TPS65552A provides three protections: thermal shutdown, max on time, and overvoltage at power SW.

Thermal Shutdown

When TPS65552A overheats, all functions stop. The only way to recover is to wait for the TPS65552A to cool down. This protection is not through *SHUTDOWN*, so the TPS65552A restarts charging if CHG stays H during the whole overheated period.

MAX ON Time

To prevent a condition such as pulling current from a poor power source (i.e., an almost empty battery), the TPS65552A provides a maximum *ON* time protection. If the *ON* time exceeds t_{MAX}, the TPS555x is forced *OFF* regardless of $I_{(PEAK)}$ detection.

Overvoltage at Power SW

To avoid the stress of power dissipation, the TPS65552A provides an overvoltage monitor function at the SW terminal. If this protection occurs, the overvoltage status is latched (see Figure 4 and its descriptions).

This function also protects short-circuit of the secondary side. In the short-circuit state of the secondary side, almost 100% of the battery voltage is supplied to SW, which stresses the device.

PCB Information

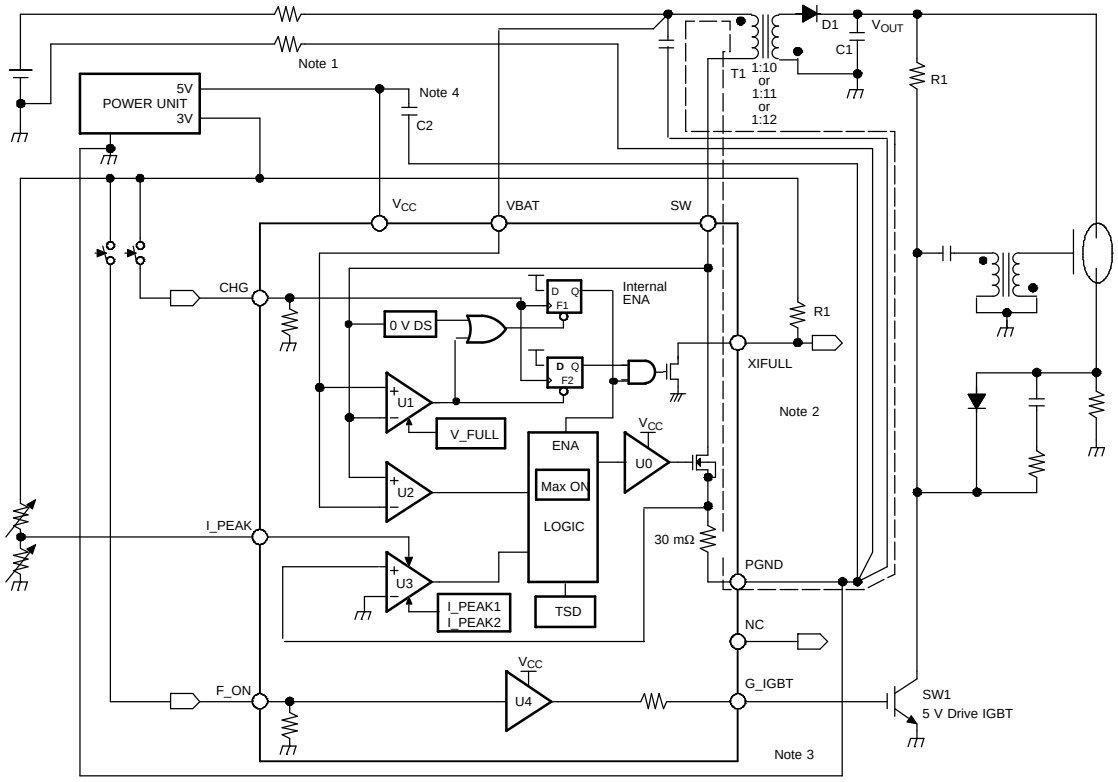


Figure 8. PCB Design Guideline(1)

(1) TI assumes no responsibility for the consequences of use of this application circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.

PRODUCT PREVIEW

Figure 8 shows key points when designing a PCB.

1. In many DSC designs, parasitic resistance that cannot be ignored, exists on the power line path from the battery to the primary side turn of the transformer. The TPS65552A has one ground point connection inside the IC at the PGND PAD. So, the PCB layout should also keep a one-point ground connection at the PGND terminal of TPS65552A.
2. The loop indicated by dotted-lines is laid out as small as possible to reduce the open area of the loop.
3. The TPS65552A uses the VCC input as a reference voltage. Considering Note 1, the ground of the *power unit* that sources VCC is connected to PGND.
4. Regarding Note 3, the bypass capacitor, C2, is required to avoid grounding noise.

Additional Technical Information

TI provides an application note for this device. For more technical information, please find the application note on the TI Web site or consult your sales contact. Literature number SLVA197.

The application note provides the following information.

1. Recommended external parts
2. PCB layout
3. Detailed operation theory
4. Calculation of the efficiency
5. Key points to design your system

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65552ADGQ	ACTIVE	MSOP-Power PAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
TPS65552ADGQG4	ACTIVE	MSOP-Power PAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
TPS65552ADGQR	ACTIVE	MSOP-Power PAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
TPS65552ADGQRG4	ACTIVE	MSOP-Power PAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
TPS65552ARGTR	ACTIVE	QFN	RGT	16	3000	Pb-Free (RoHS)	CU SN	Level-2-250C-1 YEAR
TPS65552ARGTRE3	ACTIVE	QFN	RGT	16	3000	Pb-Free (RoHS)	CU SN	Level-2-250C-1 YEAR
TPS65552ARGTT	PREVIEW	QFN	RGT	16	250	TBD	Call TI	Call TI

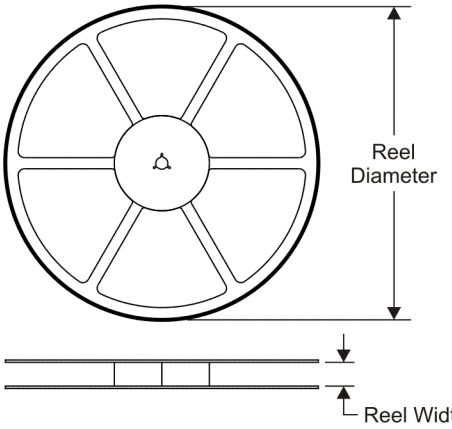
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

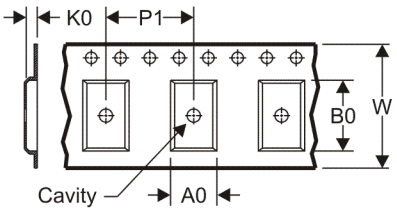
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

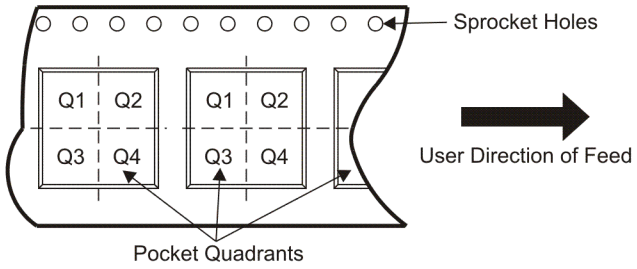


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

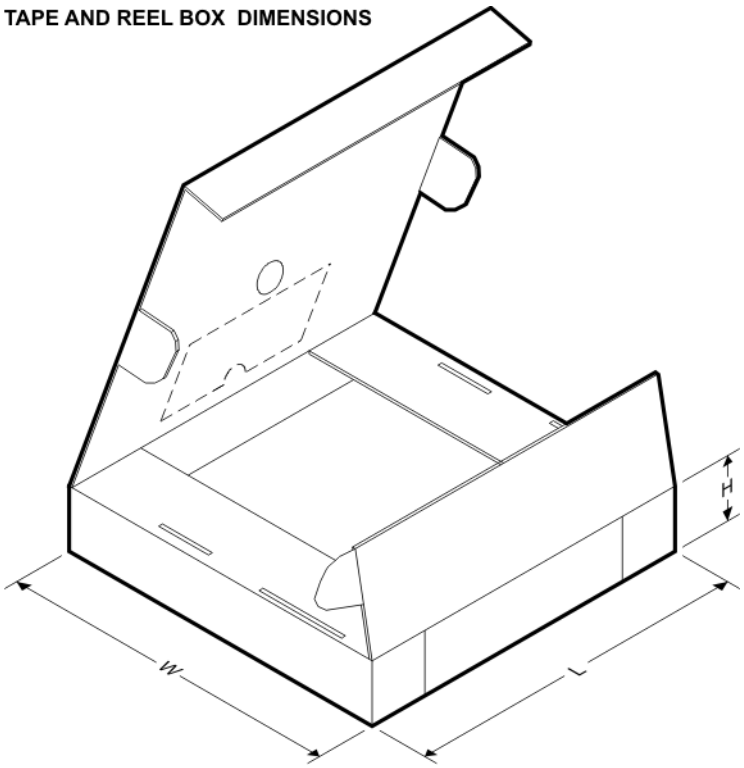
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65552ARGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

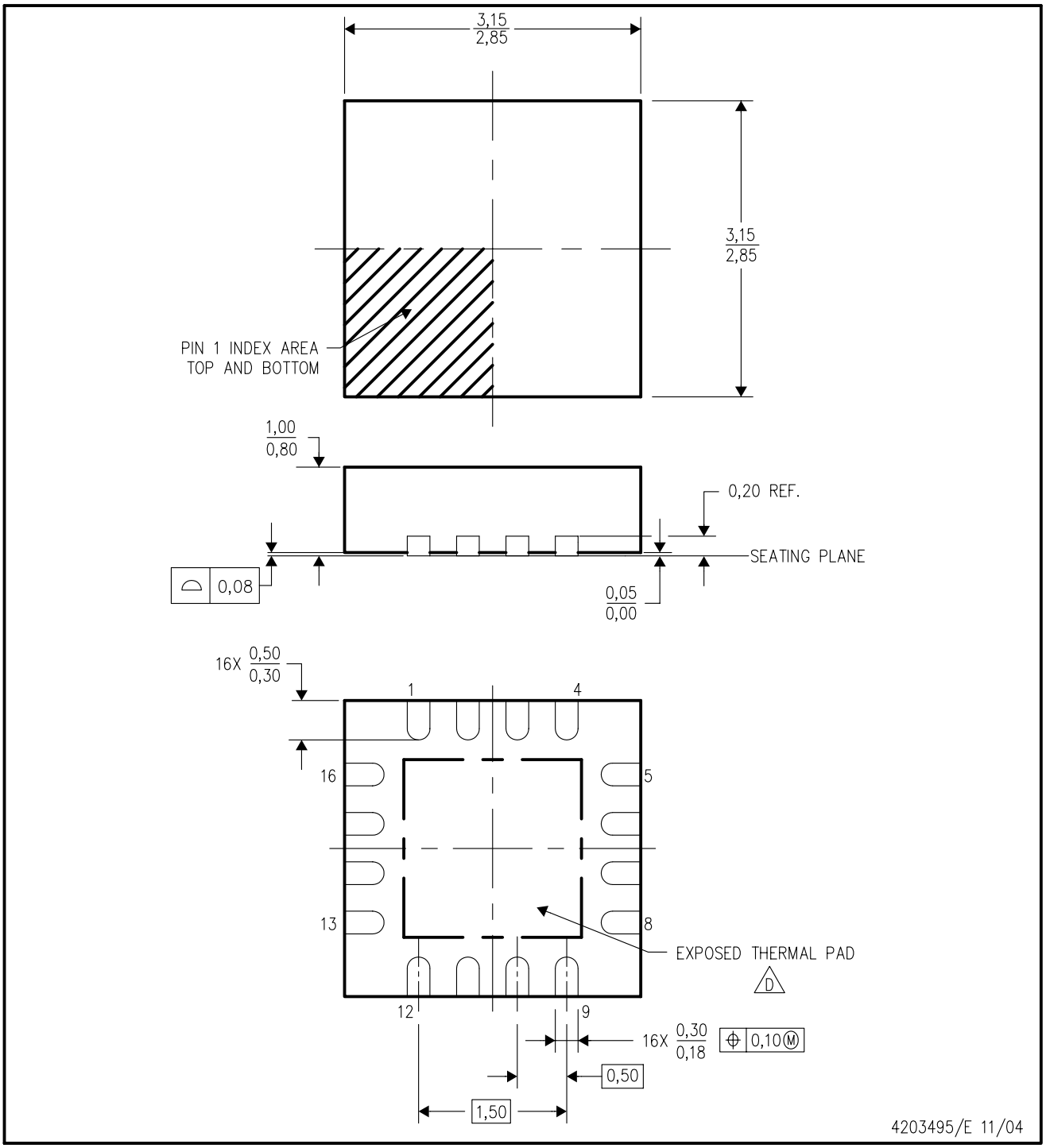
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65552ARGTR	QFN	RGT	16	3000	346.0	346.0	29.0

RGT (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

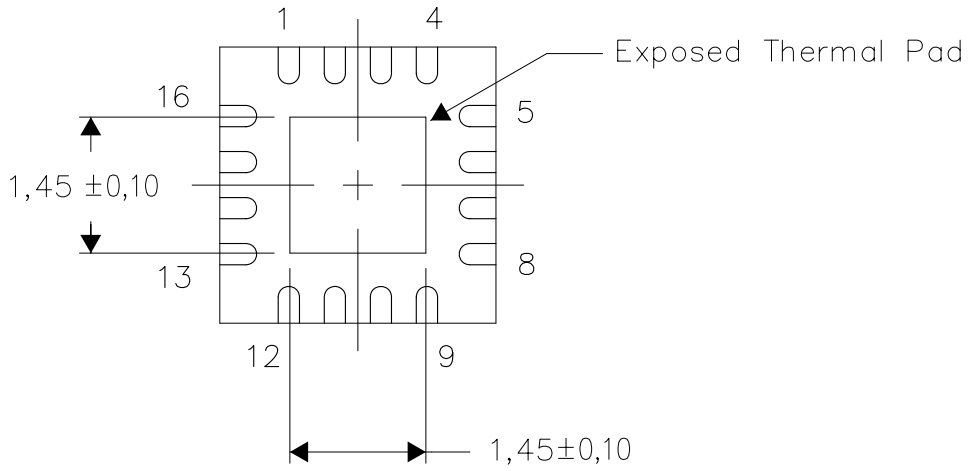
RGT (S–PVQFN–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

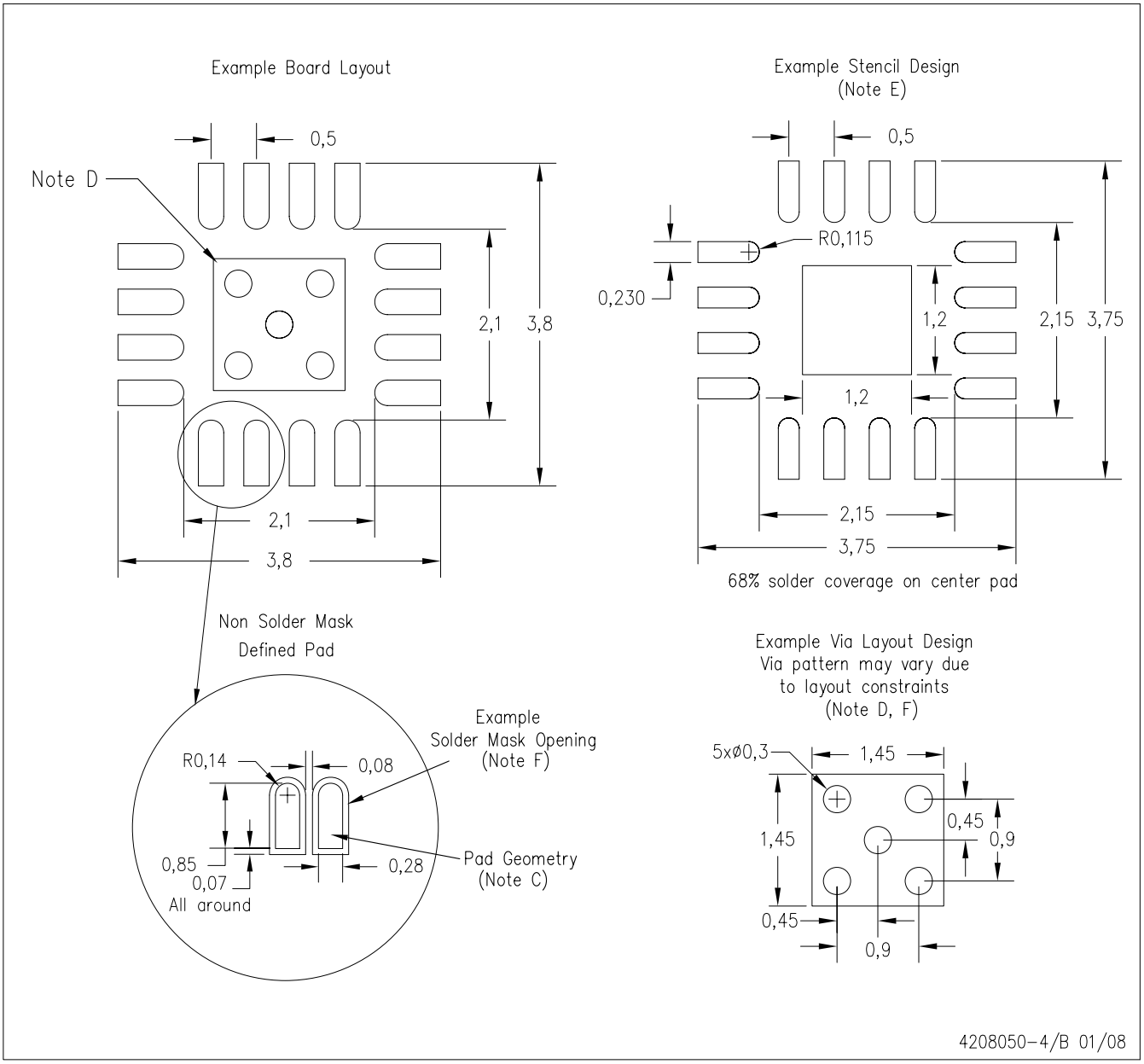


Bottom View

NOTE: All linear dimensions are in millimeters

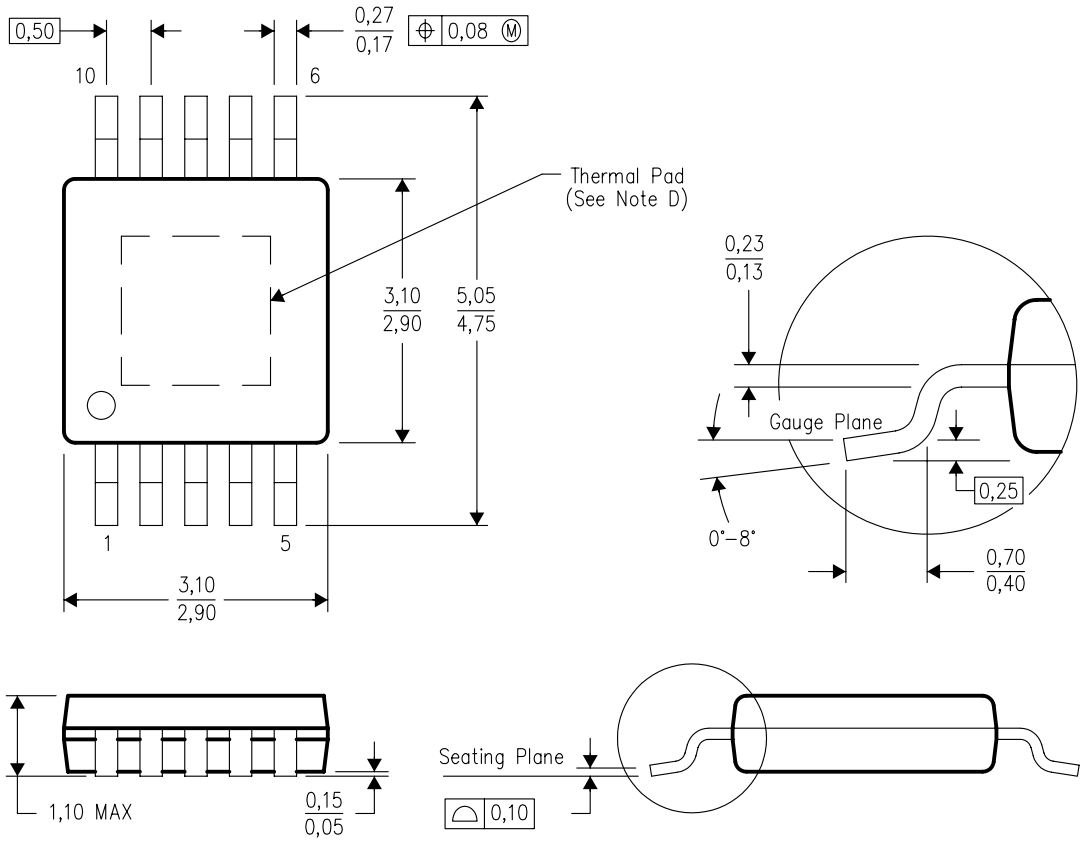
Exposed Thermal Pad Dimensions

RGT (S–PQFP–N16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187 variation BA–T.

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

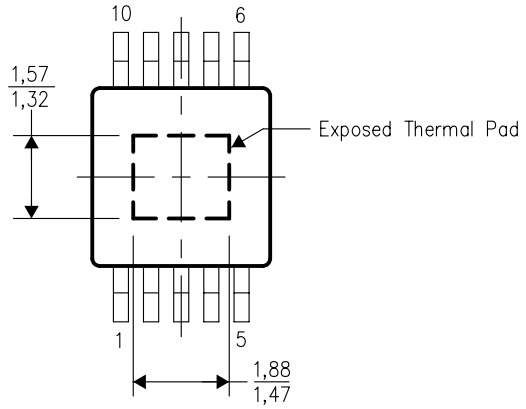
DGQ (S–PDSO–G10)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

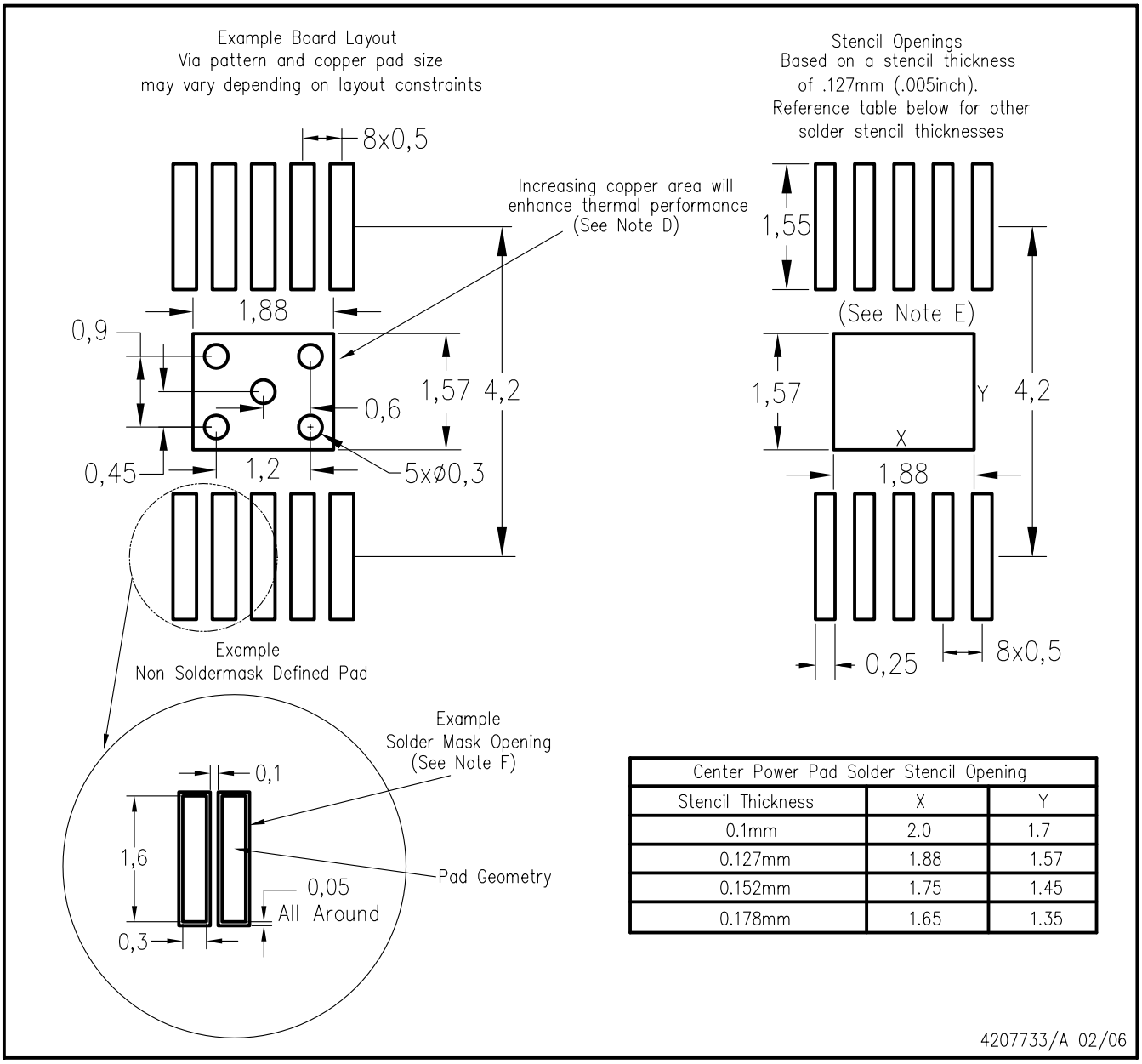


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGQ (R–PDSO–G10) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.88	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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